EARLY CAPTURE FOR BOUNDARY SCAN TIMING MEASUREMENTS

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Abstract

Analog waveforms and delays can be measured using a simple extension of the IEEE 1149.x standards. Early capture samples data on a falling edge of TMS during the Update-DR state. Experiments suggest sub-nanosecond timing resolution.

Introduction

The IEEE 1149.1 Boundary Scan Test Standard [1,2] has found wide acceptance in the test community. Boundary scan is slowly gaining converts among the circuit designers that often control the introduction of new features into system design. Unfortunately, growth has been slower than it might, as circuit designers focused on short term cost and complexity issues may not see the total system benefits of scan test. The standard is of limited applicability to some of the test problems facing test engineers. While IEEE 1149.1 provides many excellent capabilities, it has proved difficult to use for high speed testing, margin testing, and testing of mixed-signal systems [3].

The proposed P1149.4 standard [4,5] addresses mixed-signal and pin parametric issues that the purely digital IEEE 1149.1 standard cannot address. By measuring the impedances of driving buffers, for example, and inferring the threshold of receiving devices, a P1149.4 system should be able to find many of the chip-to-chip faults that may slow down a board or system. Unfortunately, P1149.4 also suffers from speed limitations, and many of the signal integrity questions that arise in high speed systems go unanswered.

Techniques involving system clock skew or frequency modification may address some of these timing issues [6], but may bring other problems. Design and test engineers may need to probe critical circuits with oscilloscopes to determine what is really happening -- or what happens with the parasitic load of an oscilloscope probe disturbing the node.

The current 1149.1 and P1149.4 standards do not address these timing issues. Signals change on boundary nets during the Update-DR state, and the Test Access Port must pass through the Select-DR state before entering the Capture-DR state to capture the results of the update. There are at least 2.5 clock cycles between the update edge and the capture edge, and the clock cycles may be need to be long if there are slow parts anywhere on the scan chain. In systems where fractions of a nanosecond may be critical, this is clearly inadequate. Some tests attempt to synchronize the optional SAMPLE instruction to the running system clock but such high-speed synchronization is difficult with most scan test systems.

This paper presents an alternative technique, which can be used as a private extension of either the 1149.1 or P1149.4 standards.

Early Capture for Digital Signals

"Early Capture" is a simple way to acquire capture inputs on selected pins during the Update-DR state. The capture may occur before, during, or after the leading edge of the Update-DR pulse, under the control of an external tester. While capturing data at times other than Capture-DR does not strictly follow the 1149.1 standard, this user instruction does not interfere with normal EXTEST and SAMPLE operations. Hopefully, this user instruction may become an optional public instruction in future versions of the 1149.x family of standards.

The early capture technique may be used with the variable-reference comparator permitted as a digitizing receiver in the emerging P1149.4 standard. By controlling both the comparator reference voltage and the timing of the early capture itself, it is possible to not only measure delays, but to digitize complete waveforms. The ability to extract waveforms may prove a powerful incentive to chip and board designers otherwise unenthusiastic about the 1149.x standards.

The Update-DR state is entered on the rising edge of TCK, and the Update-DR pulse is asserted on the falling edge of TCK. Entering Update-DR, the TMS signal is a logic one. If the next state is Select-DR, the test bus controller leaves TMS as a logic one. If the next state is Run-Test-Idle, the test bus controller drops TMS to zero, approximately around the falling edge of TCK. TMS is ignored except during the setup and hold times around the rising edge of TCK [1].

Assume the next state is Run-Test-Idle. As long as the TMS signal is stable around each rising edge of TCK, the standard allows the test controller to put the falling edge of TMS anywhere around the falling edge of TCK. The early capture technique uses this falling edge of TMS to define the sample time for the early capture latches, ahead of or behind the falling TCK edge as desired. The 1149 bus may be clocked irregularly or arbitrarily slowly to accommodate slow parts. Therefore, an Update-DR state period containing this skewed TMS edge may be arbitrarily stretched to insure adequate delays between the Update and Early Capture edges. This still allows plenty of setup and hold margin for all components in the scan chain.

If the next state is Select-DR, there will be a one on TMS at the next rising edge of TCK, with no natural downward transition. Early capture may be performed by pulsing the TMS line, returning it to a one before it is sampled at the end of Update-DR. The Update-DR state must be additionally stretched by the TMS pulse width.

TCK provides the Update or stimulus edge, and TMS provides the Capture or measurement edge. These are both downward edges, from the same controller, to an often equal number of identical loads. Whatever offsets, wiring delays, and parasitics affect one signal should affect the other equally, so relative delays should track together well (and experiments show that they do, as will be shown later). How can these two edges be used in a standard-friendly way?

To maintain strict adherence to the 1149.1 standard, all boundary cells must be able to capture input data on the rising edge of TCK at the end of the Capture-DR state. Early capture modifies some boundary cells, but in a way that does not affect their use by normal EXTEST or SAMPLE.

The early capture technique adds an additional level-sensitive latch to selected capture inputs as shown in figure 1a, with typical waveforms shown in figure 1b. Level-sensitive latches are the kind that pass data straight through when the clock is one, and hold data when the clock goes zero. These early capture latches are normally in passthrough mode, with the early capture clock one, unless the early capture instruction is selected. The latches are transparent during normal 1149.1 operation.

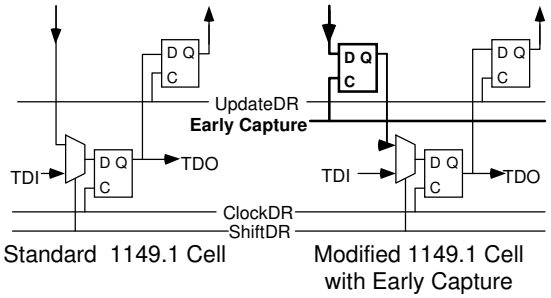

Figure 1a - Early Capture Latch

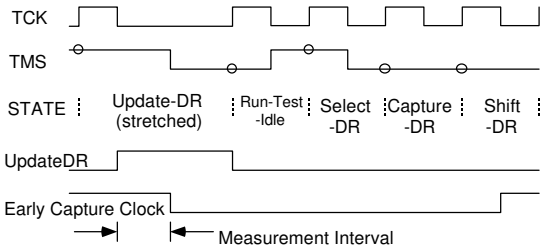

Figure 1b - Early Capture Timing

The early capture instruction behaves much like the traditional EXTEST operation, except for clocking the early capture latches into a hold state at specified times. The instruction makes the early capture clock drop from one to zero when TMS falls during the Update-DR state. This latches all early capture latches, sampling the state of the latch inputs at the falling TMS edge. The early capture clock stays low through the Capture-DR state, and returns to one during Shift-DR.

With careful design, the propagation delay through the Test Access Port can be made the same for the early capture clock and the Update-DR pulse. Thus, the delay for the two paths can be matched from the test controller through the TAP to the boundary cell. This allows tight control of the relative spacing of the two edges, even if the edges themselves are quite slow and propagation delays are long. There will be thermal noise causing timing jitter between the two paths, but this can be averaged out with repeated measurements. Residual mismatches caused by process and design variations may prove difficult to null out, but will usually be a small fraction of the normal delays in the device under test. Faster parts will tend to have smaller variations.

The initiating update event may be caused by TCK to one component, and the capturing event may occur on another component separated by a large physical distance or by many gate delays. This may cause some extra jitter in the captured signal and some error in the delay measurement. However, what usually matters in a propagation delay measurement is the relative arrival times of signals at a component, and not their relation to some arbitrary "absolute" time. Many signals may be captured at the target component at the same time. Early capture can be used to measure their relation to each other, even if their relation to some global time clock is less precisely measurable. Jitter in the arriving signal is in itself valuable test information.

Designers may choose update latches and early capture latches with opposite polarity clocks. This makes the opening edge of the update latch go in the same direction as the closing edge of the early capture latch, allowing equal gate delays from TCK and TMS. Delay errors can be made arbitrarily small with careful attention from the chip and system designers, without the need for excessively fast parts or fast scan clocks.

Controlling Edges for TCK and TMS

Early capture requires accurate control of the relative timing between the TCK and TMS signals generated by the bus controller. This is no problem for powerful test systems, but it is beyond the abilities of small 1149.x controllers and currently available bus master components. This work uses the parallel port of a DOS-compatible PC to drive the test setup. Parallel ports have a timing resolution of two microseconds -- clearly inadequate for accurate timing. However, a small amount of external circuitry can help generate adequate edges.

The test setup, shown in figure 2, uses a simple opamp based ramp generator. The parallel port of the PC generates TDI, and the precursor signals TMS* and TCK*. An additional signal, ECGATE, starts the timing ramp generator. The ramp generator drives two comparators followed by two AND gates to produce the TMS and TCK signals that drive the scan chain. The ramp generator, and the reference levels of the comparators, are driven by three outputs from a quad 12 bit DAC (Analog Devices DAC8420). The PC test controller pulses the ECGATE signal during Update-DR, starting a ramp that passes the thresholds of the TCK-EC and TMS-EC comparators in sequence. The DAC input to the ramp generator sets the slew rate, and thus the number of comparator DAC steps per microsecond.. A ramp rate of 0.61V/µsec, or 500 steps per microsecond, was chosen for this experiment.

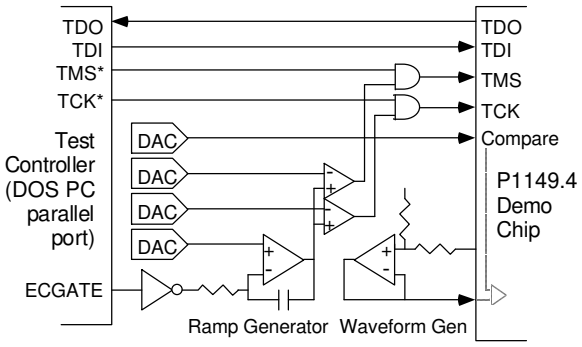

Figure 2: Waveform Measurement Test Setup

This primitive setup appears to be capable of 2 nanosecond resolution, starting with microsecond "tester" time resolution. Resolutions of tens of picoseconds should be possible with custom integration [6].

Measuring Propagation Delay

Early capture will normally be used as a production go/nogo test. The TMS edge drops at the maximum acceptable propagation delay after the TCK edge, and too-slow paths will return incorrect results. Large groups of signals, such as data or address lines, may be all measured with a single early capture operation. Minimum hold time testing is done in a similar way.

Beyond these simple tests, many modern systems require the actual measurement of propagation delay, not just minimums and maximums. For example, some components have bus outputs purposely skewed in relation to each other to minimize ground bounce. How does the test engineer verify the designer's "staggering intentions" have been met on a particular device under test? One way is to measure the propagation delay of each output directly, and early capture can be used to measure propagation delay.

Databook-style propagation delays, which are often measured to V_{IH} and V_{IL}, cannot be measured with a purely digital early capture latch with a single threshold. However, in most cases a measurement taken at the input logic threshold voltage may be adequate. The propagation delay may be found with a binary search, shifting the TMS early capture edge and looking to see if the data change occurs or not. This will require a tester or bus master that can easily change this delay between test passes.

The early capture TMS edge may be synchronized to an external clock, and used in early capture SAMPLE mode. However, digital signal early capture offers no advantages over TCK synchronization of a normal SAMPLE capture.

Analog Early Capture

This work was done as part of the demonstration chip for the P1149.4 mixed-signal extension of IEEE 1149.1. P1149.4-style interfaces on digital pins, with the variable threshold comparators permitted by P1149.4, can help us avoid the (V_{IH}/V_{IL}) quibble about propagation delay measurement. A more interesting application of early capture uses analog comparators to perform waveform extraction, rather than the simple delay measurements available for pure 1149.1 systems.

Given a repetitive signal synchronized with Update-DR, and a strobed comparator with control over both threshold and sample time, it is possible to build an equivalent-time waveform digitizer. An experimental demonstration will be described.

Each boundary module on the demonstration chip includes a zero-static-power CMOS differential comparator, taking the difference between the pin and an externally provided Compare voltage. The output of this comparator drives an otherwise unused capture bit in the module.

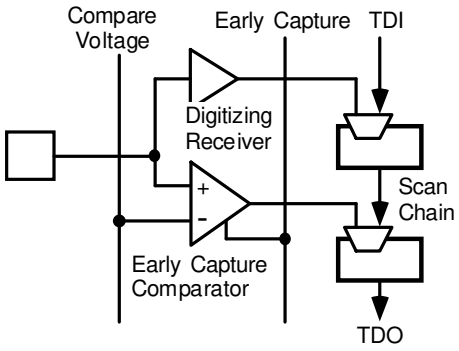

Figure 3 -Early Capture Comparator in P1149.4 Boundary Cell

The Compare voltage is driven via a separate pin by the fourth output of the previously mentioned external quad 12 bit DAC. This voltage is normally provided through the AT1 or AT2 pins of the P1149.4 test interface.

The two to three cycle delay between the early capture edge and the actual Capture-DR edge proved useful in this design to allow time for metastable comparator outputs to resolve. A linear comparator with adjustable threshold, resolving within a setup time before the Capture-DR edge, suffers from metastability and requires considerable static power. Early capture allows a simpler and cheaper design.

The early capture comparator is small and uses low dynamic power, and this causes offsets and linearity errors. However, these errors may be measured and nulled out. An error plot for a typical comparator is shown in figure 4.

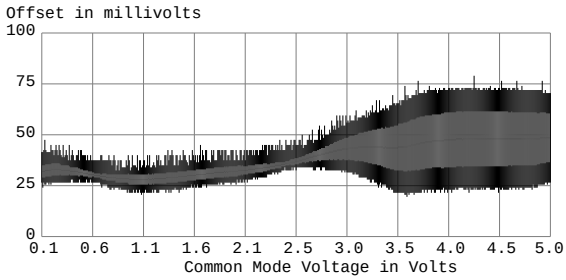

Figure 4 - Comparator Offset

The plot shows the maximum measured deviation (over twenty samples) in black, the standard deviation in gray, and the mean in black. The systematic offset and extra noise at higher common mode voltage may be minimized with a redesign of the cell.

Using the early capture timing circuitry previously described, and a variable threshold driven via the Compare input, the sample time of the early capture comparator is incremented past the update edge. At each sample time, a binary search performs twelve measurements to determine the voltage. Thus, a 500 point measurement can be made with 500 x 12 scans of the boundary, which for the demonstration chip was 45 bits long. If the initiating event is driven directly by Update-DR, twice as many scans may be required.

The demonstration experiment measures a damped sinusoid from a unity-gain-connected opamp. Because of phase delays in the opamp, a fast edge results in 1MHz ringing, making an interesting signal to sample. The edge is generated from one of the digital outputs of the demonstration chip. No effort is made to match path delays. Nonetheless, a clean waveform results, as is shown in figure 5. The horizontal axis is approximately 500 nanoseconds per division, but is not precisely calibrated.

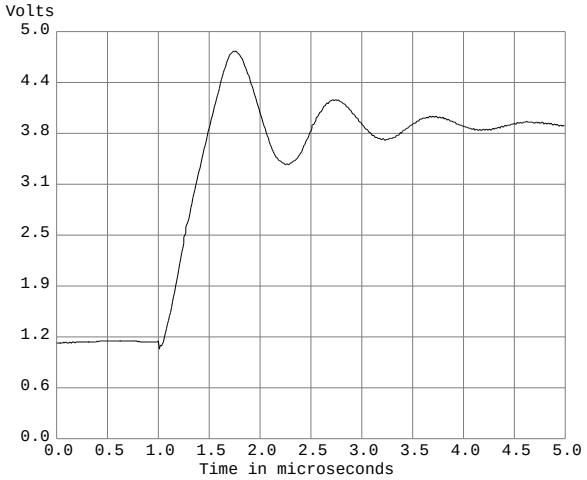

Figure 5 - Early Capture Waveform

The DAC8420's are serial input, and are driven by TCK and TDI from the PC tester; this adds to the test time. The PC using 6 microseconds to generate two TCK edges and make one sample of TDO for every "1149 clock. With additional time to save and display data, the entire waveform capture takes about 5 seconds. However, with a 10 MHz 1149 clock, separate DACs, and a 200 bit boundary length in a production test system, complete 500 point 12 bit waveforms can be generated in around 250 milliseconds. This should be adequate for gathering complete waveforms for analysis. Production "waveform envelope" tests can be made with just a few "corner samples," perhaps for many pins at once; such tests will be rapid.

The next test is more ambitious, using a gated 3 stage ECL 10K ring oscillator, with an oscillation frequency of approximately 80MHz. Analog Devices 9501 8 bit programmable delay circuits were used for the timing generator, with a full scale delay of 50 nanoseconds for this experiment. The output of this circuit was captured with the BC1 pin, and is shown below. Note the high frequency artifacts around 30 nanoseconds, which show a bandwidth for the early capture comparator well in excess of 100MHz. The overshoot in the waveform is due to mismatched termination over the 15 cm twisted pair connecting the test chip to the ECL circuit. A similar waveform appears on a 350ps sampling oscilloscope. Times are approximately nanoseconds, but not precisely calibrated.

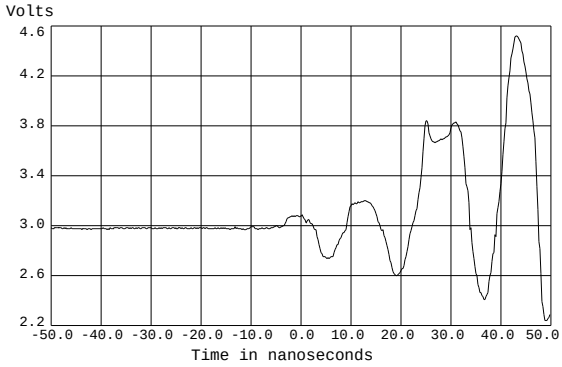

Figure 6 - ECL Ring Oscillator Startup

Yet another early capture experiment was performed with the digital early capture latches. A binary output does not yield an interesting waveform, so the ones probability is plotted instead. The time resolution for this graph is 80 picoseconds per sample point, and the probability step is quite sharp, indicating a timing jitter well under 100 picoseconds. Figure 7 shows three sample points. The first is the output of an update latch, the second is the pin waveform, and the third is the output of an external 74HC04 inverter fed back to a digital input pin. Times are in approximate nanoseconds.

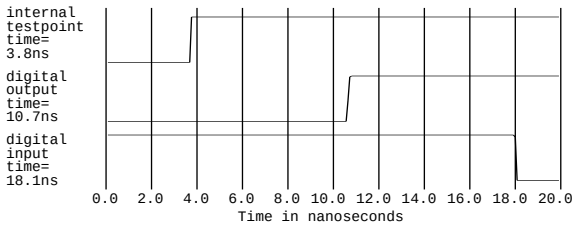

Figure 7 - Digital Waveforms

The sampling control signals pass through external gates and long wires, and the absolute delays may vary. However, the time differences between reference waveforms are repeatable and should allow accurate time measurements if the test system has accurate timing generators.

The waveform capture time may be shortened by building a non-standard one bit data register that simply reads out the result of one selected comparator. This shortens readout time to the number of BYPASSed chips following the targeted chip in the scan chain. This adds complexity more than time savings. Such complexity may be better used for separate per-pin or per-chip digitizers [7].

How fast can the analog comparator and early capture go? The demo chip uses 1.5 micron CMOS, and is assembled in a slow 40 pin dual-inline package, yet it samples waveform features well in excess of 100MHz. Faster modern processes should result in equivalently faster timing measurement.

Compatibility

Early capture may be added as a private instruction to existing 1149.1 or P1149.4 chips with no detectable effect on current tests. The early capture test instruction, and the manipulation of the TMS edge, should have no effect on existing chips. A system may be constructed of both early capture capable chips and traditional chips, with the early capture capability turned on only for the desired chips. There should be complete forward and backward compatibility with the existing standards and proposed extensions.

Conclusion

Digital early capture can perform precision time measurement with only one additional latch per pin. Analog early capture measures waveforms with a simple analog comparator that is already an optional part of the proposed P1149.4 standard. The P1149.4 bus, along with early capture, can be used as an "analog measurement superhighway" for other on-chip instruments, such as samplers, carrier detectors, temperature sensors, and so forth.

Hopefully, these additional capabilities, added to the pins of analog ICs, will make the additional cost of boundary scan palatable to engineers otherwise unconcerned about production test. Certainly they will provide the test engineer with data to design better tests, and the tools with which to implement them.

Acknowledgments

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References

[1] IEEE Standard 1149.1-1993a: "IEEE Standard Test Access Port and Boundary Scan Architecture", IEEE, 345 East 47th St., New York, NY, Oct. 1993.

[2] K. Parker, "The Boundary-Scan Handbook," Kluwer Academic Publishers, Norwell, MA, Sept. 1992.

[3] D. Josephson, D. Dixon, B. Arnold, "Test Features of the HP PA7100LC Processor", *Proceedings of the 1993 International Test Conference*, October 1993, pp. 764-72.

[4] K. Parker, J. McDermid, S. Oresjo, "Structure and Metrology for an Analog Testability Bus", *Proceedings of IEEE International Test Conference*, October 1993, pp. 309-22.

[5] B. Wilkins, editor, "P1149.4 Standard for a Mixed-Signal Test Bus", in draft.

[6] J. Maneatis, M. Horowitz, "Precision Delay Generation Using Coupled Oscillators", *IEEE Journal of Solid State Circuits,* Vol. 28, No. 12, December 1993, pp. 1273-1282.

[7] L. Whetsel, "An IEEE 1149.1 Based Voltmeter/Oscilloscope in a Chip", *VLSI Test Symposium,* April 1993, pp. 40-46.