A DEMONSTRATION IC FOR THE P1149.4 MIXED SIGNAL TEST STANDARD

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Abstract

The P1149.4 mixed-signal boundary scan standard is demonstrated with a CMOS integrated circuit. Design issues and characterization data are presented.

Introduction

The preliminary P1149.4 mixed-signal boundary scan standard [1], currently in committee, extends the IEEE 1149.1 digital boundary scan standard [2], adding analog and parametric measurement [3]. P1149.4 is intended to help automate mixed-signal board test, and reduce test interconnect, in the same way 1149.1 has.

While P1149.4 may prove useful for many kinds of testing, at minimum it provides two additional kinds of tests:

- Simple shorts-and-opens testing. All pins, input or output, may be pulled up to a VH level and down to a VL level, and all pins capture a digitizing receiver value with a threshold between these two points. This test is similar to the 1149.1 shorts-and-opens test and may use the same software.

- Two-probe parametric measurement. All pins may be connected to one or both of the on-chip global wires AB1 and AB2, which can be connected to the external test pins AT1 and AT2.

The resources to perform these tests are provided by analog boundary modules, such as the one shown in figure 1.

There are five switches shown. Switch 1 disconnects the core, so the test circuitry can control the pin. Switches 2 and 3 pull the node high or low. Switches 4 and 5 connect the pin to the AB1 and AB2 rails; switch 4 can drive the pin with a current or a voltage from AB1, and switch 5 drives voltages from the pin to the test system for measurement.

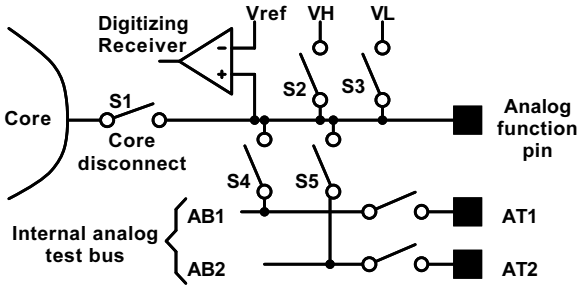


Figure 1: The Analog Boundary Module and the Bus Interface Circuit

A digitizing receiver is shown as a comparator to a reference. This may be a fixed reference, or a variable reference may be supplied via AT1 or AT2. The digitizing receiver may even be the logic input to the capture flip-flop, though this requires careful design, as will be shown.

Inputs, outputs, and bias pins all have the same five switch capabilities. This uniformity simplifies testing.

Other tests are possible using the same structure, such as routing measurements and waveforms into and out of various nodes of the device. This paper will discuss a few of the alternative tests the P1149.4 "analog measurement superhighway" makes possible.

A common misconception about P1149.4 is that all switches must be explicit in the design. Actually, all that is required is that the circuit behave **as if** the switches were there. For example, many driver circuits are already capable of powering down. All that P1149.4 requires is access to the power-down control, eliminating S1, a potentially parasitic-laden switch. Similarly, S2 and S3 may also be incorporated into the driver, as long as certain overcurrent protection limits are met. Again, this just uses the existing features of a good design.

Switches S4 and S5 may be more difficult, as processes such as bipolar do not easily allow construction of a low-leakage bi-directional switch. However, unidirectional buffers may be used instead, copying the voltage or current at AT1 to the pin, and copying the pin voltage back to AT2. The CMOS demonstration circuit did not use these work-arounds. Hopefully, a future bipolar P1149.4 demonstration circuit will test the buffer technique.

Mixed-signal systems are much harder to characterize and measure than pure digital systems. Systems with extreme high frequencies, small amplitudes, or high precision components may prove difficult to test with P1149.4. Since P1149.4 performs static tests much like 1149.1, some non-static or feedback dependent circuits may also be hard to test. Initially, P1149.4 will not solve every test problem, but it will provide a stable, transportable base on which many new test techniques can be developed.

Designing Analog Boundary Modules

A test standard is intended to act as an interface between the chip designer, the board designer, the test engineer, the test software programmer, and the test equipment manufacturer. A properly designed standard will guide the silicon designer to provide the on-chip and specification resources necessary so the other participants can do their jobs. A standard that allows the chip designer to produce boundary modules that are not useful for test is no standard at all -- it is a waste of time and chip area.

Analog boundary modules are implemented with real transistors, with significant parasitic resistance and capacitance. Transistors have voltage and current limits that can put severe limits on testing. The transistors must also be protected from electrostatic discharge, and ESD protection circuits, if designed improperly, can cause P1149.4 metrology problems.

The digitizing receiver may have a fixed threshold. If the threshold chosen cannot be reached by the circuit under test, the digitizing receiver is rendered useless. This may be a particular problem for standard parts with a wide range of uses, and a variable threshold may prove more useful.

Unlike the digital 1149.1 boundary cell, which must simply pass ones and zeros to predefined logic levels, a P1149.4 boundary module contains many design decisions about switch sizes, voltage ranges, thresholds, and so forth. These decisions must be made on the basis of the test envisioned for the circuitry connected to that module. If the pin is capable of driving many watts into an 8 ohm load at audio frequencies, different design tradeoffs will be made than for a pin that connects to a GHz RF input. It may be difficult to design boundary module switches for parts with a wide range of uses.

Choosing Switches

MOS transistor conductivity is proportional to channel width, but so is the junction capacitance. Transistors robust enough to handle pin ESD often have longer channels and wider diffusions than transistors in the core, resulting in much higher capacitance-to-conductivity ratios at the periphery. Since ESD does not scale with technology, the capacitance-to-conductivity ratio of an advanced short-channel process may be the same or worse than the ratio for an older, longer channel process.

For example, the maximum typical drain capacitance divided by the minimum typical switch conductance for a PMOS/NMOS device pair constructed with the TSMC 1.2 micron process is typically about 80 picoseconds, and is dominated by PMOS behavior. The TSMC 0.6 micron process has a capacitance-to-conductivity ratio of around 90 picoseconds. The device models yielding these results are proprietary to TSMC, but other manufacturer's data will probably have similar results. The ratio may double in the worst case.

Chip designers must choose transistors with conductivity high enough to drive external circuitry, but capacitance low enough to avoid seriously degrading bandwidth. This makes the choice of transistor widths difficult.

The purpose of board short circuit testing is to locate shorts, not to destroy the components

connected to the short. Thus the VH and VL switches must be able to survive large voltage differences. This may require increased switch area and channel length to spread out device heating.

Once the switch designs are chosen, there must be some way to describe switch parasitics and limitations to the test software so it can automatically choose the voltages, currents, and pathways used for test. Different pins on the same component will have different tradeoffs, and each switch performs a different mission, so every pin may need separate descriptions for each switch.

The P1149.4 demonstration chip contains boundary module switches ranging from 180 ohms to 14K ohms, measured at nominal supply and room temperature.

ESD Protection Resistors

A common form of ESD protection circuit is the resistor pi connection, shown in figure 2a.

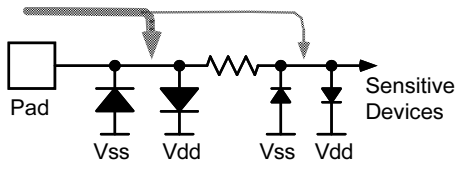


Figure 2a: ESD Protection Circuit with Resistor

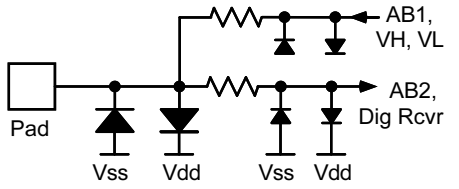


Figure 2b: Two Resistors Needed for Accurate AB2, Digitizing Receiver Voltage Measurement

ESD currents flow through the outer diodes; the currents are large enough to put large voltages across the diodes. The resistor and the inner diodes limit the voltage on the inner node to levels that short-channel internal devices can tolerate.

The protection resistor can be a problem for metrology. If a measurement current is injected to the node through this resistor, the voltage drop across it will invalidate voltage readings at the protected end. Therefore, the AB2 voltage sensing switch, and the digitizing receiver, must be connected to a separate protection resistor and set of internal diodes, as shown in figure 2b. The common path through contacts, internal wiring, and the bond wire should be minimized as well, and may need to be characterized for the test measurement software.

Digitizing Receiver Design

The digitizing receiver can be a subtle source of difficulty. In CMOS, the most obvious digitizing receiver is a simple inverter, but these are not suitable because of their interaction with analog signals. Normally, an analog signal on the input to such a circuit would keep both the P and N channel transistors in the inverter turned on, resulting in an undesirable standing current between the power supplies. Further, if the inverter is biased near its threshold, Miller capacitance from output to input will "kick back" charge into the input, causing noise and signal distortion.

The demonstration chip uses two kinds of digitizing receivers. One is a "zero static power analog comparator" consisting of input switches, a switched cross-coupled pair, and output isolators to balance the load on the cross-couple and isolate the analog signals on it from the digital circuitry downstream. This comparator is shown in figure 3.

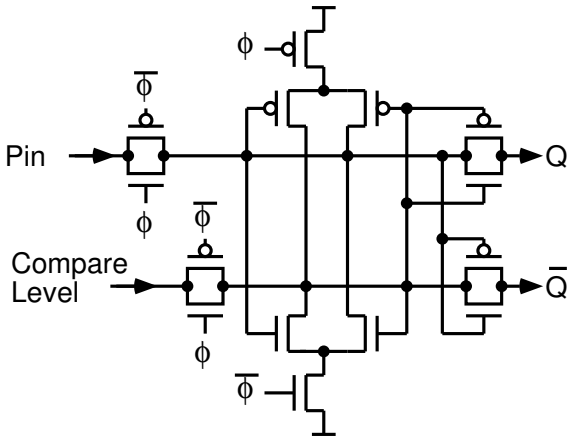


Figure 3: Zero Static Power Comparator

This circuit draws current from the supplies only briefly, when it transitions from follower to latching mode. However, the signal-side storage node, and thesources of the transistors connected to it, are a nonlinear parasitic load on the signal.

Also, the input switches will inject some charge into the input when the cell is latched. After latching, some time is required to settle from sampling to latched mode, or offsets may occur. This comparator may develop offsets from charge trapping in the cross-coupled transistors, so a third precharge state may be desirable for highest accuracy. The four isolation transistors minimize output loading effects when the comparator is near balance.

The other "digitizing receiver" used on the demo chip is a logic input, but not an inverter. Instead, the input drives a transfer-gate multiplexor into a capture flip-flop on the boundary chain. The transfer gate connects the input gates of the flip-flop to the analog signal node, but only during EXTEST when TCK is low in the Capture-DR state. Thus, the logic is normally disconnected from the pin. However, the operation of the boundary register, even during SAMPLE, may temporarily corrupt signals on P1149.4 pins. Designers should consider signal isolation circuitry if this is a problem.

The Demonstration Integrated Circuit

Unlike IEEE 1149.1, based on a large body of prior boundary scan experience, P1149.4 began with a concept -- extending boundary scan to mixed signal systems. Many plausible concepts may prove impractical when subjected to real world scrutiny, while many of the feared problems may vanish when confronted with persistent engineering effort. As part of an effort to move the P1149.4 standard from the conceptual to the practical, the working group began work on a demonstration chip in 1994.

The P1149.4 demonstration integrated circuit is a full custom, cell based design. It was made with IMP Semiconductor's 1202 CMOS process, using 1.5 micron drawn devices. The demo chip was assembled in a 40 pin dual inline package.

A block diagram of the demonstration chip is shown in figure 4. The circuit contains a Test Access Port identical to the 1149.1 digital TAP. The rest of the chip consists of various test structures to explore the effects of the P1149.4 boundary module on both on-chip and external circuitry.

The demonstration circuits on the P1149.4 demo chip are:

- Four boundary modules, with different bit order and switch styles. A fifth module using a peculiar control scheme was included, but proved non-functional.
- Two large 50 ohm, 100MHz amplifiers, one with boundary modules and one without. The otherwise identical amplifiers are differential and have a special differential measurement bus.
- Internal test structures for measuring thresholds and currents - a "virtual process monitor".
- AT bus interface switches. Since the RF amplifiers are differential, a differential **four** wire measurement bus was used, rather than normal two wire analog measurement bus. The two extra test pins for differential measurement will not be needed in most cases.
- A digital input and output pin pair, with normal 1149.1 testability.

The boundary chain connects all the pins at the interface, along with single-bit switch controls for the internal cells. The total boundary data register is 45 bits long.

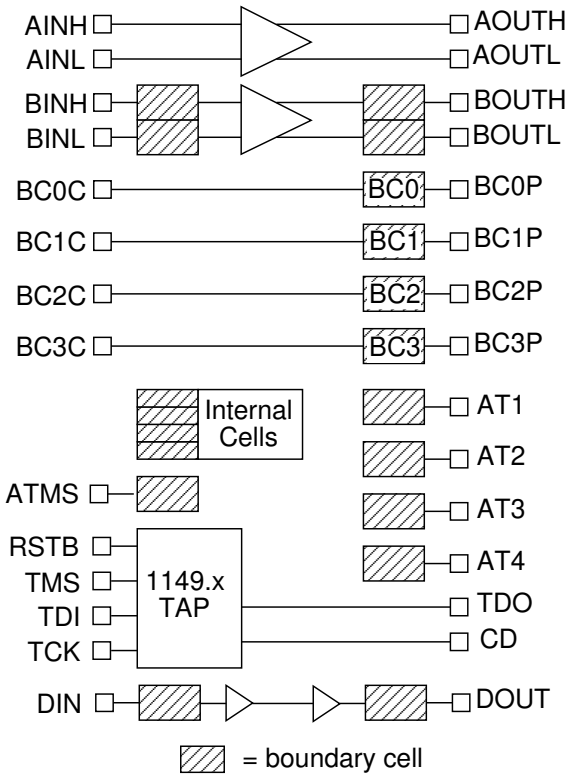


Figure 4: Demo Chip Block Diagram

The Boundary Modules

The four boundary modules tested various design approaches, and are numbered BC0 through BC3. All modules have two pins, a "pin" side and a "core" side on the other end of a 200 ohm core disconnect switch. Questions affecting boundary module implementation include:

- Should there be protection resistors, or should the transistors be given large junctions and longer channels for ESD protection?
- Should each switch S2-S5 have a separate control bit, or should switches decode from three control bits?
- If the control bits are decoded, should this be done with logic gates, or by constructing switches out of transistors in series to combine the logic signals?
- What is the effect of switch sizing on layout?

A complete answer to these questions could result in hundreds of modules; the demo chip contains just the following four:

- BC0 uses a 3 bit control register with decoders. The module states are decoded without gates, rather by two or three transistors in series. The transistors are large ESD-proof transistors with 2 micron long, 12 micron wide channels.
- BC1 also uses series decoding, and has smaller transistors protected by two ESD resistors.
- BC2 is the most practical module, with gate decoding from three control bits and single ESD-proof transistors for switches.
- BC3 uses a separate control bit for each switch, resulting in a four bit boundary module. However, some gating is still necessary to allow MODE to control the module.

There are also four boundary modules on the input and the output of the amplifier. The switches between ATx and ABx have also been characterized, and add in series with the switch resistances of the other modules. The switch resistances in ohms of the six kinds of modules are shown in table 1.

	AB1	AB2	VL	VH
BC0	5300	3500	1900	6500
BC1	13400	9000	5500	1700
BC2	1700	1600	670	2200
BC3	1700	1600	670	2200
AMPx	200	370	180	500
ATx	90	90	670	2200

Table 1: Boundary Cell Switch Resistances

The AT switches are larger and less resistive than the others. These switches disconnect the AB lines from the AT lines on the board, reducing leakage and capacitance on those lines to that of a single connected part. The parasitic capacitance of these switches does not affect mission pins, so they can be large.

One lesson learned from the layout of the boundary switches is to minimize the number of wires connecting the switches to the logic and update cells. The switches using series transistor gating took more room than the logic gate driven switches due to the inconvenience of routing wires into the guard-ringed switch areas.

Virtual Process Monitors

With the analog measurement system in place, it is tempting to use it for other purposes besides boundary testing. One promising and profitable use of the P1149.4 interface is embedded process characterization circuits.

Part of the manufacturing of semiconductor wafers is the inclusion of process monitors, groups of transistors with separate pads that are probed on the wafer to characterize it. Process monitors usually consist of about a dozen transistors, some strings of contacts, resistors of various shapes and layers, and a small sea of probe pads so a tester can get at them all. The process monitor is either stepped separately instead of the useful die on the wafer, or placed in the scribe grid and stepped with every die. In either case, the process monitor is a compromise between adequate process information and the large expanse of pads necessary to connect all the different devices.

P1149.4 can help eliminate separate process monitors, and can provide better wafer tests with significant wafer area savings. By placing test devices inside the chip and connecting them with

AB1 and AB2, they can be significantly smaller than probe pads. Devices may be selected by decoding in an X-Y grid, and on-chip current sensors can measure the results. Small but sophisticated circuits can be designed to extract inferred process variables like gate threshold. Other test circuitry can mimic the critical portions of the mission circuitry on the die. On-chip measurement circuitry can be calibrated and controlled from off chip. Finally, all this circuitry can be disabled via a fusible link or other programming bit, allowing semiconductor foundries to protect their process data.

To completely demonstrate this concept would take a large design effort. As a simple illustration, the demo chip incorporates four simple measurements that might be on such a test key. Two diode-connected transistors, one for P channel and one for N channel, allow estimation of current characteristics. The three-transistor cell shown in figure 5 generates a voltage approximating the process threshold voltage.

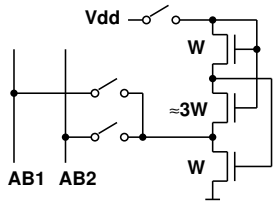


Figure 5: VT Measurement Circuit

Other circuits, generating currents or voltages proportional to mobility, oxide thickness, and other parameters can be envisioned. With appropriate design of test circuitry, process characterization may be no more difficult than connecting a P1149.4 tester and measuring DC values.

The diode-connected N-channel transistor device demonstrated the importance of appropriate switch sizing, because the AB1 switch was too small and resistive. N-channel transistors are more conductive than P-channel transistors, and the P-channel device in the switch provides most of the test current. The N-channel diode barely turns on before the AB1 switch current limits, making measurements difficult. This illustrates the need for careful choice of device sizes for switches.

Other Tests

The demo chip instruction register is 8 bits long, with bits controlling which tests are enabled and which are not, allowing the P1149.4 working group to choose appropriate mandatory instructions from among the many possibilities.

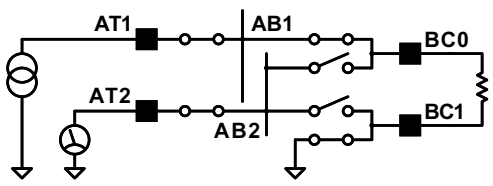
The amplifier bandwidth was measured with boundary cells and without them. The boundary cells included an explicit series core-disconnect switch. An explicit switch is unnecessary in a real design since the amplifier can be turned off, but is included here to measure parasitic degradation. The impact was serious; bandwidth was reduced from 140MHz to 60MHz, and gain was reduced from 3.15 to 2.95. It is critical that designers use cell power-down rather than series core-disconnect switching wherever possible.

The demo chip incorporates two other features: "analog TMS" and "early capture." The analog TMS scheme [4] connects the internal AB1 line to a modified TMS line during Run-Test-Idle, potentially eliminating the need for the AT1 test pin and reducing the cost of the P1149.4 interface. This feature is enabled by setting one of the instruction bits, and connecting the ATMS pin to TMS with a jumper -- if such a feature were standardized the connection would be made on-chip to one pad. However, incompatibilities with the existing 1149.1 standard preclude its use for P1149.4.

Early capture [5] uses a downward edge on TMS during Update-DR to generate a sampling edge, allowing data to be captured very quickly after the Update-DR edge, even with slow clocks. This technique allows accurate timing measurements and the sampling of analog waveforms. Early capture is used to strobe the zero-static-power comparators described above, and is supported with a control bit and four extra gates in the TAP and instruction register.

Parametric Extraction of External Circuits

The P1149.4 demonstration chip was used to perform a simple resistor measurement as shown below:



A 200µA (±0.3uA) current was used to measure a 1000.87 ohm resistor. The current travels through the AT1 pin and AT1 switch, through the

AB1 switch to the BC0 pad, through the external resistor, and back into the chip through the BC1 pad, where it travels to ground through the VL or ground guard switch. Voltage is measured at either BC0 or BC1 via the AB2 bus to the meter on AT2; the voltage measurement is switched back and forth between the pins under boundary scan control.

The current was generated by an opamp-controlled discrete PNP circuit, and drifted during measurement. The current was measured with a Fluke 8502A 5.5 digit DVM, and the voltages were measured with a Data Precision 2440 5.25 digit DVM. The voltage at the AT1 pin was 2.2395V (±0.5mV). The voltage at AT2 connected to BC0 was 1.4780V, and 1.2786V connected to BC1. The difference voltage of 199.4mV results in a resistance measurement of 997 ohms, well within experimental error for this rather noisy setup. More accuracy is possible with a higher accuracy current source and better signal averaging. Apparent switch resistances are higher than those given in Table 1; the voltage across the switches is high enough to start saturating the transistors, and causes noticeable self-heating. Lower measurement voltages and currents are suggested, if the measurement circuitry permits it.

The demonstration circuit above illustrates two additional effects the switch designer should pay attention to. The VL switch voltage drop may be quite large compared to the resistance of the external component being tested. The voltage drop is a function of both device temperature and the gate voltage of the switch transistor. If the device has significant current through it, it will self heat, and cause the common-mode voltage across the resistor to drift during measurement. This is not a large problem if a true differential voltage measurement is being made, but it can affect the accuracy of the pseudo-differential sequential measurements that P1149.4 makes. The switch resistance is also a function of the driving voltage on the gate of the VL transistor. If the gate is connected to a noisy digital supply, that noise will be amplified and cause common mode errors. Both these effects may be minimized with a large, low resistance switch.

Conclusion

The success of P1149.4 will depend on the proper design of components supporting it. The boundary modules on these components must be designed with careful attention to parasitics, ESD, and metrology, and must be well characterized for the test software. The P1149.4 bus can also be used to connect other structures for testing, such as test devices or internal test nodes.

Acknowledgments

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